Integrated Circuit Systems, Inc.

# ICS9248-150

## Frequency Generator for Multi-Processor Servers

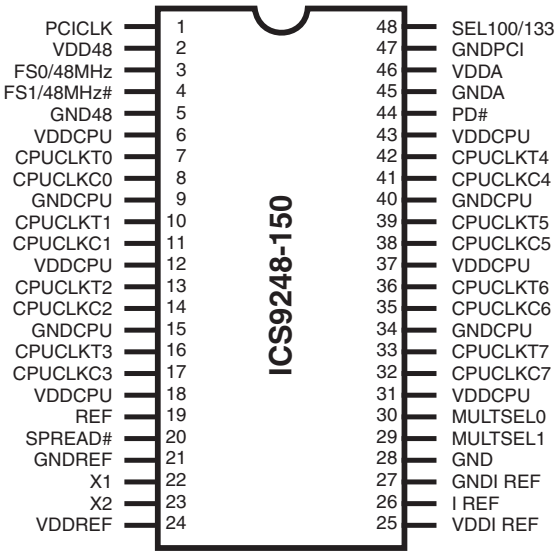
**Recommended Application:**
ServerWorks Grand Champion Systems

**Output Features:**
- 8 - Differential CPU Clock Pairs @ 3.3V
- 1 - 3V 33MHz PCI clocks
- 1 - 48MHz clock
- 1 - Inverted 48MHz clock
- 1 - 14.318MHz reference output

**Features:**
- Up to 200MHz frequency support
- Support power management: Power Down Mode
- Supports Spread Spectrum modulation: 0 to -0.5% down spread.
- Uses external 14.318MHz crystal
- Select logic for Differential Swing Control, Test mode, Tristate, Power down, Spread Spectrum.
- External resistor for current reference
- FS pins for frequency select

**Key Specifications:**
- PCI Output jitter <500ps
- CPU Output jitter <150ps
- 48MHz Output jitter <350ps
- REF Output jitter < 1000ps

### Pin Configuration




**48-Pin SSOP and TSSOP**

### Functionality

| SEL133/100 | FS0 | FS1 | Function |
|---|---|---|---|
| 0 | 0 | 0 | Active 100MHz |
| 0 | 0 | 1 | 100MHz Test Mode |
| 0 | 1 | 0 | 100MHz Test Mode |
| 0 | 1 | 1 | Tristate all outputs |
| 1 | 0 | 0 | Active 133MHz |
| 1 | 0 | 1 | 133MHz Test Mode |
| 1 | 1 | 0 | Active 200MHz |
| 1 | 1 | 1 | Reserved |

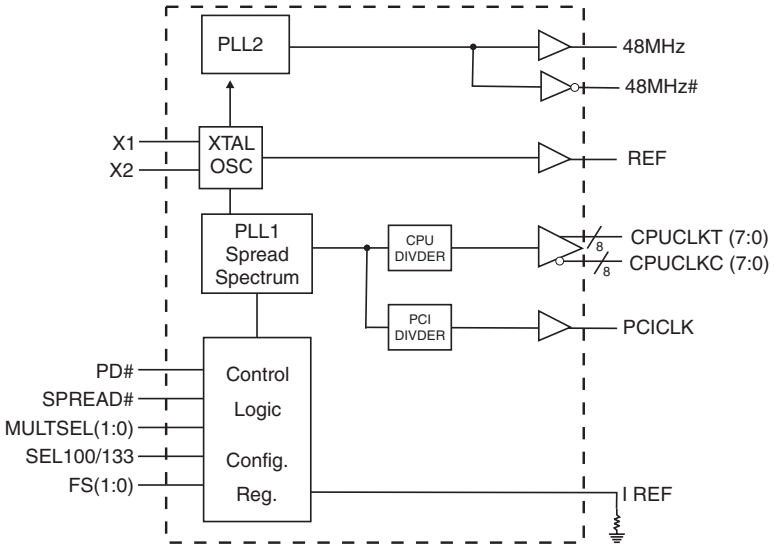
### Analog Power Groups

VDD48, GND48 = 48MHz, PLL2
VDDA=VDD (core supply voltage 3.3V)
GNDA=Ground for core supply

### Digital Power Group

VDDREF, GNDREF = REF, Xtal

### Block Diagram



## General Description

**ICS9248-150** is a main clock for ServerWorks Grand Champion Systems.
Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. **ICS9248-150** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

## Pin Configuration

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | PCICLK | OUT | PCI clock output |
| 2, 6, 12, 18, 24, 31, 37, 43, | VDD | PWR | 3.3V power supply |
| 3 | FS0 | IN | Frequency select pin |
| | 48MHz | OUT | 48MHz clock output |
| 4 | FS1 | IN | Frequency select pin |
| | 48MHz# | OUT | Inverted 48MHz clock output |
| 5, 9, 15, 21, 28, 34, 40, 47 | GND | PWR | Ground pins for 3.3V supply |
| 33, 36, 39, 42, 16, 13, 10, 7 | CPUCLKT (7:0) | OUT | "True" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias. |
| 32, 35, 38, 41, 17, 14, 11, 8 | CPUCLKC (7:0) | OUT | "Complementary" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias. |
| 19 | REF | OUT | Reference output 14.318MHz |
| 20 | SPREAD# | IN | Invokes Spread Spectrum functionality on the Differential host clocks, Active Low |
| 22 | X1 | X2 Crystal Input | 14.318MHz Crystal input |
| 23 | X2 | X1 Crystal Output | 14.318MHz Crystal output |
| 25, 46 | VDDI REF VDDA, | PWR | Analog power supply 3.3V |
| 26 | I REF | OUT | This pin establishes the reference current for the CPUCLK pairs. This pin takes a fixed precision resistor tied to ground in order to establish the required current. |
| 29, 30 | MULTSEL(1:0) | IN | CPU swing select inputs |
| 44 | PD# | IN | Invokes power-down mode. Active Low. |
| 27, 45 | GNDI REF GNDA | PWR | Analog Ground pins for 3.3V supply |
| 48 | SEL100/133 | IN | CPU Frequency Select. Low=100MHz, High=133MHz |

## Truth Table

| SEL 133/100 | FS0 | FS1 | CPUCLK MHz | PCICLK MHZ | 48 MHz |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 100 | 33 | 48 |
| 0 | 0 | 1 | 100 | 33 | Disable |
| 0 | 1 | 0 | 100 | Disable | Disable |
| 0 | 1 | 1 | Tristate | Tristate | Tristate |
| 1 | 0 | 0 | 133 | 33 | 48 |
| 1 | 0 | 1 | 133 | 33 | Disable |
| 1 | 1 | 0 | 200 | 33 | 48 |
| 1 | 1 | 1 | TCLK/2 | TCLK/8 | TCLK/2 |

## CPUCLK Buffer Configuration

| | Conditions | Configuration | Load | Min | Max |
|---|---|---|---|---|---|
| **Iout** | Vdd = nominal (3.30V) | All combinations of M0, M1 and Rr shown in table below | Nominal test load for given configuration | -7% I nominal | +7% I nominal |
| **Iout** | Vdd = 3.30 ± 5% | All combinations of M0, M1 and Rr shown in table below | Nominal test load for given configuration | -12% I nominal | +12% I nominal |

## CPUCLK Swing Select Functions

| MULTSEL0 | MULTSEL1 | Board Target Trace/Term Z | Reference R, Iref= Vdd/(3*Rr) | Output Current | Voh @ Z, Iref=2.32mA |
|---|---|---|---|---|---|
| 0 | 0 | 60 ohms | Rr = 475 1% Iref = 2.32mA | Ioh = 5*Iref | 0.71V @ 60 |
| 0 | 0 | 50 ohms | Rr = 475 1% Iref = 2.32mA | Ioh = 5*Iref | 0.59V @ 50 |
| 0 | 1 | 60 ohms | Rr = 475 1% Iref = 2.32mA | Ioh = 6*Iref | 0.85V /2 60 |
| 0 | 1 | 50 ohms | Rr = 475 1% Iref = 2.32mA | Ioh = 6*Iref | 0.71V @ 50 |
| 1 | 0 | 60 ohms | Rr = 475 1% Iref = 2.32mA | Ioh = 4*Iref | 0.56V @ 60 |
| 1 | 0 | 50 ohms | Rr = 475 1% Iref = 2.32mA | Ioh = 4*Iref | 0.47V @ 50 |
| 1 | 1 | 60 ohms | Rr = 475 1% Iref = 2.32mA | Ioh = 7*Iref | 0.99V @ 60 |
| 1 | 1 | 50 ohms | Rr = 475 1% Iref = 2.32mA | Ioh = 7*Iref | 0.82V @ 50 |
| | | | | | |
| 0 | 0 | 30 (DC equiv) | Rr = 221 1% Iref = 5mA | Ioh = 5*Iref | 0.75V @ 30 |
| 0 | 0 | 25 (DC equiv) | Rr = 221 1% Iref = 5mA | Ioh = 5*Iref | 0.62V @ 20 |
| 0 | 1 | 30 (DC equiv) | Rr = 221 1% Iref = 5mA | Ioh = 6*Iref | 0.90V @ 30 |
| 0 | 1 | 25 (DC equiv) | Rr = 221 1% Iref = 5mA | Ioh = 6*Iref | 0.75V @ 20 |
| 1 | 0 | 30 (DC equiv) | Rr = 221 1% Iref = 5mA | Ioh = 4*Iref | 0.60 @ 20 |
| 1 | 0 | 25 (DC equiv) | Rr = 221 1% Iref = 5mA | Ioh = 4*Iref | 0.5V @ 20 |
| 1 | 1 | 30 (DC equiv) | Rr = 221 1% Iref = 5mA | Ioh = 7*Iref | 1.05V @ 30 |
| 1 | 1 | 25 (DC equiv) | Rr = 221 1% Iref = 5mA | Ioh = 7*Iref | 0.84V @ 20 |

## Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to $V_{DD}$ +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A$ = 0 - 70°C; Supply Voltage $V_{DD}$ = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | | 2 | | $V_{DD}$ + 0.3 | V |
| Input Low Voltage | $V_{IL}$ | | $V_{SS}$ - 0.3 | | 0.8 | V |
| Input High Current | $I_{IH}$ | $V_{IN} = V_{DD}$ | -5 | | 5 | mA |
| Input Low Current | $I_{IL1}$ | $V_{IN}$ = 0 V; Inputs with no pull-up resistors | -5 | | | mA |
| | $I_{IL2}$ | $V_{IN}$ = 0 V; Inputs with pull-up resistors | -200 | | | |
| Operating Supply Current | $I_{DD3.3OP}$ | $C_L$ = 0 pF; Select @ 100 MHz | | 181 | 250 | mA |
| Powerdown Current | $I_{DD3.3PD}$ | $C_L$ = 0 pF; Input address to VDD or GND | | 52 | 60 | mA |
| Input Frequency | $F_i$ | $V_{DD}$ = 3.3 V | | 14.318 | | MHz |
| Pin Inductance | $L_{pin}$ | | | | 7 | nH |
| Input Capacitance[1] | $C_{IN}$ | Logic Inputs | | | 5 | pF |
| | $C_{OUT}$ | Output pin capacitance | | | 6 | pF |
| | $C_{INX}$ | X1 & X2 pins | 27 | | 45 | pF |
| Clk Stabilization[1, 2] | $T_{STAB}$ | CPU Freq. = 100/133 MHz | | | 8 | ms |
| | | CPU Freq. = 200 MHz | | | 10.5 | ms |
| Clk Recovery[1, 3] | $T_{REC}$ | CPU Freq. = 100/133 MHz | | | 8 | ms |
| | | CPU Freq. = 200 MHz | | | 10.5 | ms |
| Delay[1] | $t_{PZH}$,$t_{PZL}$ | Output enable delay (all outputs) | 1 | | 10 | ns |
| | $t_{PHZ}$,$t_{PLZ}$ | Output disable delay (all outputs) | 1 | | 10 | ns |

[1]Guaranteed by design, not 100% tested in production.

[2]From VDD = 3.3V to 1% of target frequency

[3]From deassertion of PD# to 1% of target frequency

## Electrical Characteristics - CPU

$T_A$ = 0 - 70°C; VDD=3.3V +/-5%; $C_L$ = 10-20 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output Impedance | $R_{DSP2B}$[1] | $V_O = V_{DD}*(0.5)$ | | 714 | | Ω |
| Output Impedance | $R_{DSN2B}$[1] | $V_O = V_{DD}*(0.5)$ | | 714 | | Ω |
| Output High Voltage | $V_{OH2B}$ | $I_{OH}$ = -1 mA | 2 | | | V |
| Output Low Voltage | $V_{OL2B}$ | $I_{OL}$ = 1 mA | | | 0.4 | V |
| Output High Current | $I_{OH2B}$[2] | $V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 2.375 V | -27 | | -27 | mA |
| Output Low Current | $I_{OL2B}$[2] | $V_{OL@MIN}$ = 1.2 V, $V_{OL@MAX}$ = 0.3 V | 27 | | 30 | mA |
| Rise Time | $t_{r2B}$[1] | $V_{OL}$ = 20%, $V_{OH}$ = 80% | 175 | 324 | 700 | ps |
| Fall Time | $t_{f2B}$[1] | $V_{OH}$ = 80%, $V_{OL}$ = 20% | 175 | 501 | 700 | ps |
| Diff. Crossover Volta | $V_x$ | $V_{DD}$ = 3.3V | 45 | 50 | 55 | % |
| Duty Cycle | $d_{t2B}$[1] | $V_T$ = 50% | 45 | 51.2 | 55 | % |
| Skew CPUT0:7 | $t_{sk2B}$[1] | $V_T$ = 50% | | 83.8 | 100 | ps |
| Skew CPU C0:7 | $t_{sk2B}$[1] | $V_T$ = 50% | | 78.5 | 100 | ps |
| Jitter | $t_{jcyc-cyc}$[1] | $V_T$ = 50% | | 86 | 150 | ps |

[1]Guaranteed by design, not 100% tested in production.

[2] $I_{OWT}$ can be varied and is selectable thru the MULTSEL pin.

## Electrical Characteristics - REF

$T_A$ = 0 - 70°C; VDD=3.3V +/-5%; $C_L$ = 10-20 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output Frequency | $F_{O1}$ | | | 14.318 | | MHz |
| Output Impedance | $R_{DSP1}$[1] | $V_O = V_{DD}*(0.5)$ | 20 | 48 | 60 | Ω |
| Output High Voltage | $V_{OH}$[1] | $I_{OH}$ = -1 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL}$[1] | $I_{OL}$ = 1 mA | | | 0.4 | V |
| Output High Current | $I_{OH}$[1] | $V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V | -29 | | -23 | mA |
| Output Low Current | $I_{OL}$[1] | $V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V | 29 | | 27 | mA |
| Rise Time | $t_{r1}$[1] | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 1 | 1.6 | 4 | ns |
| Fall Time | $t_{f1}$[1] | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 1 | 2.4 | 4 | ns |
| Duty Cycle | $d_{t1}$[1] | $V_T$ = 1.5 V | 45 | 53.5 | 55 | % |
| Skew | $t_{sk1}$[1] | $V_T$ = 1.5 V | | | N/A | ps |
| Jitter | $t_{jcyc-cyc}$[1] | $V_T$ = 1.5 V | | 305 | 1000 | ps |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - PCI

$T_A$ = 0 - 70°C; VDD=3.3V +/-5%; $C_L$ = 10-30 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output Frequency | $F_{O1}$ | | | 33.3 | | MHz |
| Output Impedance | $R_{DSP1}$[1] | $V_O = V_{DD}*(0.5)$ | 12 | 33 | 55 | Ω |
| Output High Voltage | $V_{OH}$[1] | $I_{OH}$ = -1 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL}$[1] | $I_{OL}$ = 1 mA | | | 0.55 | V |
| Output High Current | $I_{OH}$[1] | $V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V | -33 | | -33 | mA |
| Output Low Current | $I_{OL}$[1] | $V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V | 30 | | 38 | mA |
| Rise Time | $t_{r1}$[1] | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 0.5 | 1.2 | 2 | ns |
| Fall Time | $t_{f1}$[1] | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 0.5 | 1.2 | 2 | ns |
| Duty Cycle | $d_{t1}$[1] | $V_T$ = 1.5 V | 45 | 49.9 | 55 | % |
| Skew | $t_{sk1}$[1] | $V_T$ = 1.5 V | | | N/A | ps |
| Jitter | $t_{jcyc-cyc}$[1] | $V_T$ = 1.5 V | | 139.7 | 500 | ps |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - 48MHz

$T_A$ = 0 - 70°C; VDD=3.3V +/-5%; $C_L$ = 10-20 pF (unless otherwise specified)

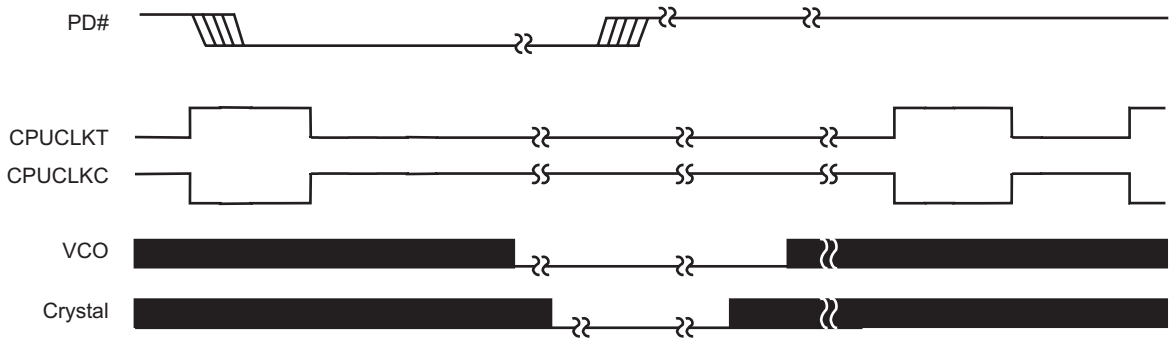
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output Frequency | $F_{O1}$ | | | 48 | | MHz |
| Output Impedance | $R_{DSP1}$[1] | $V_O = V_{DD}*(0.5)$ | 20 | 48 | 60 | Ω |
| Output High Voltage | $V_{OH}$[1] | $I_{OH}$ = -1 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL}$[1] | $I_{OL}$ = 1 mA | | | 0.4 | V |
| Output High Current | $I_{OH}$[1] | $V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V | -29 | | -23 | mA |
| Output Low Current | $I_{OL}$[1] | $V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V | 29 | | 27 | mA |
| Rise Time | $t_{r1}$[1] | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 1 | 1.3 | 4 | ns |
| Fall Time | $t_{f1}$[1] | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 1 | 1.6 | 4 | ns |
| Duty Cycle | $d_{t1}$[1] | $V_T$ = 1.5 V | 45 | 52.5 | 55 | % |
| Skew | $t_{sk1}$[1] | $V_T$ = 1.5 V | | | N/A | ps |
| Jitter | $t_{jcyc-cyc}$[1] | $V_T$ = 1.5 V | | 175 | 350 | ps |

[1]Guaranteed by design, not 100% tested in production.

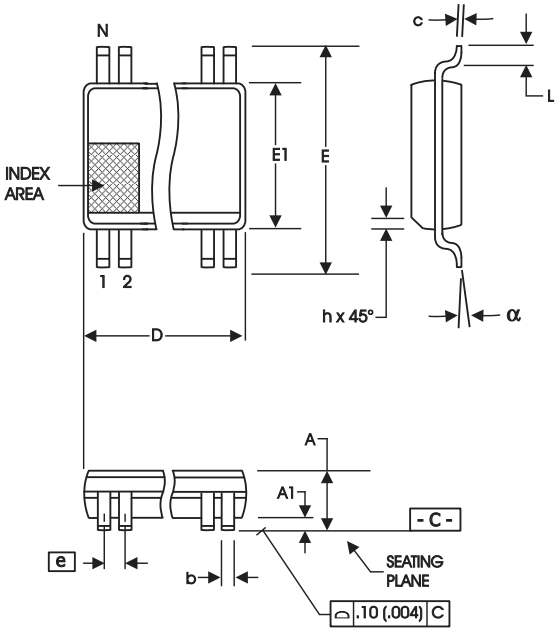
## PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power down latency should be as short as possible but conforming to the sequence requirements shown below.




**Notes:**
1. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
3. The shaded sections on the VCO and the Crystal signals indicate an active clock.




**300 mil SSOP Package**

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.41 | 2.80 | .095 | .110 |
| A1 | 0.20 | 0.40 | .008 | .016 |
| b | 0.20 | 0.34 | .008 | .0135 |
| c | 0.13 | 0.25 | .005 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 10.03 | 10.68 | .395 | .420 |
| E1 | 7.40 | 7.60 | .291 | .299 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| h | 0.38 | 0.64 | .015 | .025 |
| L | 0.50 | 1.02 | .020 | .040 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 48 | 15.75 | 16.00 | .620 | .630 |

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

## Ordering Information

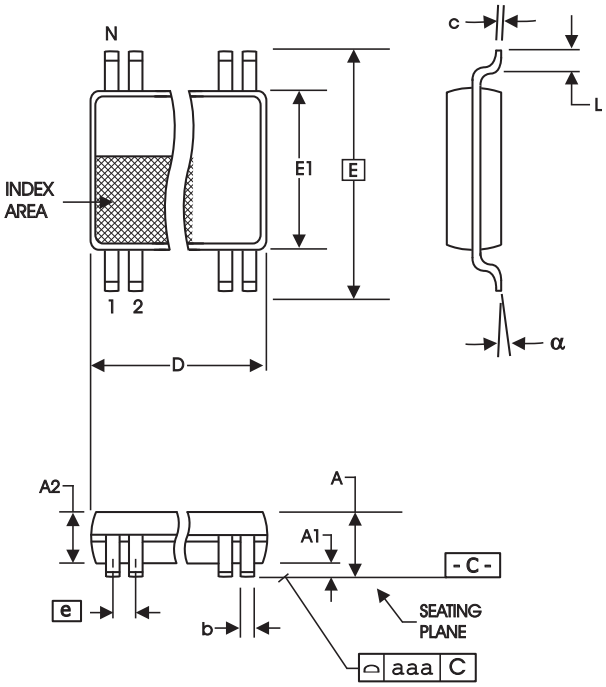
**ICS9248yF-150-T**

Example:

**ICS XXXX y F - PPP - T**

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS, AV = Standard Device

0352E—06/09/05




| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.17 | 0.27 | .007 | .011 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 8.10 BASIC | | 0.319 BASIC | |
| E1 | 6.00 | 6.20 | .236 | .244 |
| e | 0.50 BASIC | | 0.020 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

'ARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 48 | 12.40 | 12.60 | .488 | .496 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

**6.10 mm. Body, 0.50 mm. pitch TSSOP**
**(240 mil) (0.020 mil)**

## Ordering Information

**ICS9248yG-150-T**

Example:

**ICS XXXX y G - PPP - T**

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  G=TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS, AV = Standard Device

0352E—06/09/05

## Revision History

| Rev. | Issue Date | Description | Page # |
|---|---|---|---|
| E | 6/9/2005 | Removed PCI Skew from Electrical Characteristics Table. | 7 |
| | | | |
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| | | | |